Sheet 1 of 1

Form PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 728-236 (YOR9 2003 0149 US1)	SERIAL NO. 10/620,734
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	APPLICANTS Sameh W. Asaad et al.	
	FILING DATE July 16, 2003	GROUP ART UNIT 2183

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
LS		6,401,196	06/04/02	Lee et al.			

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

		LS 1.	N. Bellas, I. Hajj and C. Polychronopoulos, in "A New Scheme for I-Cache Energy Reduction In High-Performance Processors," Power Driven Microarchitecture Workshop, held in conjunction with ISCA 98, Barcelona, Spain, June 28th 1998.
		LS 2.	K. Ghose and M. B. Kamble, in "Energy Efficient Cache Organizations for Superscalar Processors," Power Driven Microarchitecture Workshop, held in conjunction with ISCA 98, Barcelona, Spain, June 28th 1998.
		LS 3.	J. Kin, M. Gupta and W. Mangione-Smith, "The Filter Cache: An Energy Efficient Memory Structure," Proc. Int'l Symposium on Microarchitecture, pp. 184-193, December, 1997
		LS 4.	C. Su, A. M. Despain, in "Cache Design Tradeoffs for Power and Performance Optimization: A Case Study," Proc. Int'l Symposium on Low Power Design, pp. 63-68, 1995.
		LS 5.	L.H. Lee, W. Moyer and J. Arends, "Instruction Fetch Energy Reduction Using Loop Caches for Embedded Applications with Small Tight Loops," Proc. Int'l Symp on Low Power Design, 1999.

EXAMINER	DATE CONSIDERED
[signature]	1/3/06

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.